What is claimed is:

1. An integrated circuit capable of supporting a plurality of host processor families, comprising:

   a host processor belonging to a first processor family;

   a reconfigurable processor core coupled to the host processor, the reconfigurable processor core having a core portion processing instructions belonging to a second host processor family; and

   a processor type select circuit to configure the integrated circuit to process instructions belonging to one of the first or second host processor family instruction set.

2. The circuit of claim 1, wherein the first host processor family comprises a processor compatible with an ARM processor family.

3. The circuit of claim 1, wherein the second host processor family comprises a processor compatible with a MIPS processor family.

4. The circuit of claim 1, further comprising an analog portion integrated on the substrate, including:

   a cellular radio core;

   a radio sniffer coupled to the cellular core; and

   a short-range wireless transceiver core coupled to the cellular core.

   a digital portion integrated on the substrate, including:

5. The circuit of claim 4, wherein the reconfigurable processor core is coupled to the cellular radio core and the short-range wireless transceiver core, the reconfigurable processor adapted to handle a plurality of wireless communication protocols.

6. The circuit of claim 4, further comprising a high-density memory array core coupled to the reconfigurable multi-processor core.

7. The wireless device on a single substrate of claim 1, wherein the protocol conforms to a Bluetooth™ or IEEE802.11 protocol.

8. The wireless device on a single substrate of claim 1, wherein the protocol software conforms to a Global System for Mobile Communications (GSM) protocol.

9. The wireless device on a single substrate of claim 1, wherein the protocol software conforms to a General Packet Radio Service (GPRS) protocol.

10. The wireless device on a single silicon substrate of claim 1, wherein the protocol software conforms to an Enhance Data Rates for GSM Evolution (Edge) protocol.

11. The wireless device on a single substrate of claim 1, wherein the reconfigurable processor core includes one or more digital signal processors (DSPs).

12. The wireless device on a single substrate of claim 1, wherein the reconfigurable processor core includes one or more reduced instruction set computer (RISC) processors.

13. The wireless device on a single substrate of claim 1, further comprising a router coupled to the processor, the cellular radio core, and the short-range wireless transceiver core.

14. The wireless device on a single substrate of claim 13, wherein the router further comprises an engine that tracks the destinations of packets and send them in parallel through a plurality of separate pathways.

15. The wireless device on a single substrate of claim 13, wherein the router sends packets in parallel through a primary and a secondary communication channel.